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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/873,242	06/05/2001	Haruo Kamimaki	ASA-1008	5964

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EXAMINER	
DANG, KHANH	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 02/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/873,242	KAMIMAKI ET AL.	
	Examiner	Art Unit	
	Khanh Dang	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20041206*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

In claim 8, it is unclear whether the "transfer number register" is a single part of a "data transfer controller" or is included in the "transfer number counting unit."

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-8, 10-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Mitsushira et al.

At the outset, it is first noted that similar claims will be grouped together to avoid repetition in explanation. It is also noted that it has been held that the recitation that an element is "capable of" performing a function is not a positive limitation but only requires the ability to so perform. It does not constitute a limitation in any patentable sense. *In re Hutchison*, 69 USPQ 138.

As broadly drafted, these claims do not define any structure that differs from Mitsuhira et al. With regard to claim 1, Mitsuhira et al. discloses a data transfer controller comprising: an initial value register (address register 208/209, for example), a transfer start address (initial address) of a transfer source or transfer destination being initially set to the initial value register (208/209, for example) from an external; and a control unit (DMA Controller 205 including DMA Execution Control Unit 200) which requests an interrupt to the external each time data transfer responding to a transfer request from the external reaches a predetermined data amount (upon completion of a predetermined DMA transfer) when data transfer based upon the transfer start address (initial address), and initializes an address of the transfer source or transfer destination to the transfer start address in said initial value register each time the interrupt is issued a plurality of predetermined times (or in another word, in Mitsuhira et al., each time DMA transfer is executed and an interrupt is issued thereafter, the value at the terminal counter 205 is decreased. When the counter 205 reaches 0 after a predetermined of times or counts or in another word, after a number of issued interrupts, the data transfer of all data in the DMA transfer area is completed. Upon completion of DMA transfer for the number specified for one DMA transfer area, the data transfer control device using DMA updates the initial address of the next DMA transfer and the number of transfers for the next DMA transfer area). With regard to claim 2, see above explanation regarding claim 1. It is also clear that it is clear that the device of Mitsihira et al. is a semiconductor device and the DMA controller 205 including Execution Control Unit 200 is an arithmetic and logic controller. With regard to claim 3, see explanation above

regarding to claim 1. It is also clear that it is clear that the device of Mitsihira et al. is a semiconductor device and the DMA controller 205 including Execution Control Unit 200 is an arithmetic and logic controller. Mitsuhira et al also discloses RAM 103 to store DMA transfer area before an interrupt is issued; and peripheral circuit 104. With regard to claim 4, Misihira st al. discloses a data transfer controller comprising: an initial value register (address register 208, for example) capable of being externally set with transfer control address information; an address counting unit (address update unit 207, for example) which renews the transfer control address information each time data is transferred from a transfer source to a transfer destination; a temporary address register (209, for example) to which the transfer control address information set to the initial value register is set, the set transfer control address information being sequentially renewed by the address counting unit; a transfer number counting unit (terminal counter 205) capable of repetitively performing an operation of counting the number of transfer times up to a first target number each time data is transferred from the transfer source to the transfer destination; a repetition number (area counter 701, for example) capable of repetitively performing an operation of counting the number of repetition times of the operation of the transfer number counting unit which counts the number of transfer times up to the first target number, up to a second target number; and a control unit (DMA controller 205 including Execution Control Unit 200) which starts a data transfer operation from the transfer source to the transfer destination in response to a data transfer request, outputting an interrupt signal each time the transfer number counting unit counts the first target number, and setting the transfer control address information

to the temporary register from the initial value register each time the repetition number counting unit counts the second target number. With regard to claims 5 and 6, it is clear from Mitsuhira et al. and the above explanation that the temporary address register 209 is capable of being either a destination address register or a source address register, since data transfer between peripheral 101 and RAM 103 is bi-directional. With regard to claim 7, as best the Examiner can ascertain from the language of the claim, the temporary address register 209, depending from the transfer direction, can be a source address register when data is transferred one way, or a "destination address register" when data is transferred the other way; and the DMA controller 205 including Execution Control Unit 200 may select either one to start a data transfer control. With regard to claim 8, it is clear that the transfer number counting unit (terminal counter 205) includes a counter (register) which can be externally set with a so-called "first target number." With regard to claim 10, the RAM 103 is used as a transfer source or transfer destination. With regard to claims 11 and 12, see explanation above regarding at least claims 1-4. With regard to claims 13 and 14, see explanation provided above. In addition, it is clear that the RAM 130 and the DMA Controller 105 is formed in a single unit 150. It is also clear that unit 150 is a semiconductor device. In any event, the method of forming a device is not germane to the issue of patentability of the device itself. The newly added limitation is fully address under Response to Argument.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mitsuhira et al.

Mitsuhira et al., as discussed above, discloses the claimed invention including the use of a so-called "second target number." However, Mitsuhira et al. does not specifically disclose that the "target number is three." It would have been obvious to one of ordinary skill in the art at the time the invention was made to select a specific target number for Mitsuhira et al., since such a selection is merely a matter of design choice. In any event, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2D 272, 205 USPQ 215 (CCPA 1980).

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mitsuhira et al.

Mitsuhira et al., as discussed above, discloses the claimed invention including the use a peripheral (101) connected to I/O circuit (there must be an I/O circuit in Mitsuhira et al. so that the peripheral 101 can be connected to). However, Mitsuhira et al. does not specifically disclose that the peripheral (101) is a voice/sound signal input

circuit. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a voice/sound signal input as a peripheral (101) in Mitsuhira et al. for providing Mitsuhira et al. with multimedia setting, since the Examiner takes Official Notice that the use of voice/sound signal input as a peripheral or I/O device in a digital multimedia setting is old and well-known in the art as evidenced from at least Wood et al. (cited below as supportive evidence); and only involves routine skill in the art.

Response to Arguments

Applicants' arguments filed 12/06/2004 have been fully considered but they are not persuasive.

At the outset, Applicants are reminded that claims subject to examination will be given their broadest reasonable interpretation consistent with the specification. *In re Morris, 127 F.3d 1048, 1054-55 (Fed. Cir. 1997).* In fact, the "examiner has the duty of police claim language by giving it the broadest reasonable interpretation." *Springs Window Fashions LP v. Novo Industries, L.P.,* 65 USPQ2d 1862, 1830, (Fed. Cir. 2003). Applicants are also reminded that claimed subject matter not the specification, is the measure of the invention. Disclosure contained in the specification cannot be read into the claims for the purpose of avoiding the prior art. *In re Sporck*, 55 CCPA 743, 386 F.2d, 155 USPQ 687 (1986).

With this in mind, the discussion will focus on how the terms and relationships thereof in the claims are met by the references. Response to any limitations that are not

in the claims or any arguments that are irrelevant and/or do not relate to any specific claim language will not be warranted.

The 112, 2nd paragraph Rejection:

With regard to claim 8, Applicants' amendment and remark have not clarified the issue whether the "transfer number register" is a single part of a "data transfer controller" or is included in the "transfer number counting unit."

The Mitsuhira et al. 102 Rejection :

Applicants argue that Mitsuhira et al. does not disclose "overwriting data to the initialized specified area." Contrary to Applicants' argument, DMA Controller (205) including DMA Execution Control Unit (200) requests an interrupt to the external each time data transfer responding to a transfer request from the external reaches a predetermined data amount upon completion of a predetermined DMA transfer when data transfer based upon the transfer start address (initial address), and initializes an address of the transfer source or transfer destination to the transfer start address in said initial value register each time the interrupt is issued a plurality of predetermined times. In another, in Mitsuhira et al., each time DMA transfer is executed and an interrupt is issued thereafter, the value at the terminal counter (205) is decreased. When the counter (205) reaches 0 after a predetermined of times or counts or in another word, after a number of issued interrupts, the data transfer of all data in the DMA transfer area is completed. Upon completion of DMA transfer for the number specified for one DMA

transfer area (reaching an end address of a particular data transfer area or destination), the data transfer control device using DMA **updates (see at least column 3, lines 35-44; column 4, lines 13-22).** The initial address of the next DMA transfer and the number of transfers for the next DMA transfer area (to continuously transfer data after reaching an end address of a particular transfer area or destination). See at least column 3, line 32 to column 4, line 24; column 7, lines 16-52; and column 8, lines 57-62. **The mere fact that data in the initialized specified area is updated indicates "overwriting data to the initialized specified area."**

The Mitsuhira 103 Rejection:

Applicants did not separately argued against the 103 Rejection.

Any inquiry concerning this communication should be directed to Khanh Dang at telephone number 703-308-0211.

Khanh Dang
Primary Examiner